#### DISCRETE SEMICONDUCTORS

# DATA SHEET

### **BSP121**

# N-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of April 1995
File under Discrete Semiconductors, SC13b

1998 Apr 01





#### **BSP121**

#### **DESCRIPTION**

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

#### **FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

#### **QUICK REFERENCE DATA**

Drain source voltage	V <sub>DS</sub>	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	350 mA
Total power dissipation up to			
T <sub>amb</sub> = 25 °C	$P_{tot}$	max.	1.5 W
Drain-source on-resistance $I_D = 400 \text{ mA}$ ; $V_{GS} = 10 \text{ V}$	R <sub>DS(on)</sub>	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance $I_D = 400 \text{ mA}; V_{DS} = 25 \text{ V}$	Y <sub>fs</sub>	min. typ.	200 mS 350 mS

#### **PINNING - SOT223**

1 = gate

2 = drain

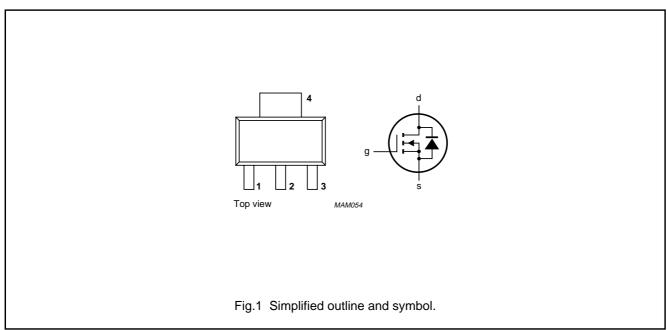
3 = source

4 = drain

#### Marking code

BSP121

#### **PIN CONFIGURATION**



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### N-channel enhancement mode vertical D-MOS transistor

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#### **RATINGS**

Limiting values in accordance with the	Absolute Maximum System (IEC 134)
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Drain-source voltage	$V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{\sf GSO}$	max.	20	V
Drain current (DC)	$I_{D}$	max.	350	mΑ
Drain current (peak)	I <sub>DM</sub>	max.	1.2	Α
Total power dissipation up to				
$T_{amb} = 25 ^{\circ}C \text{ (note 1)}$	$P_{tot}$	max.	1.5	W
Storage temperature range	$T_{stg}$	-65 to	+ 150	°C
Junction temperature	T <sub>i</sub>	max.	150	°C

#### THERMAL RESISTANCE

From junction to ambient (note 1)  $R_{thj-a} = 83.3 \text{ K/W}$ 

#### Note

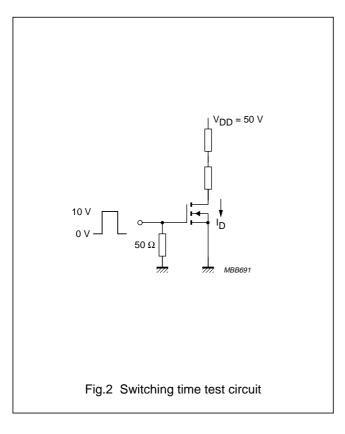
<sup>1.</sup> Device mounted on an epoxy printed-circuit board 40 mm  $\times$  40 mm  $\times$  1.5 mm; mounting pad for the drain lead min. 6 cm<sup>2</sup>.

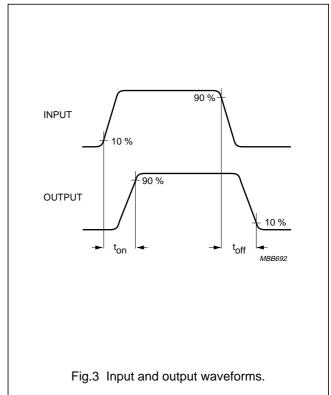
### N-channel enhancement mode vertical D-MOS transistor

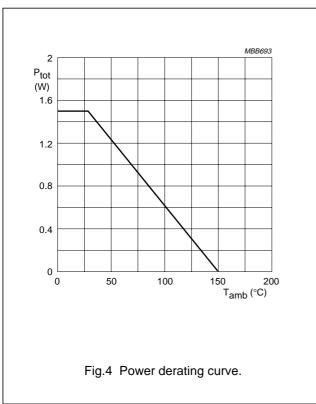
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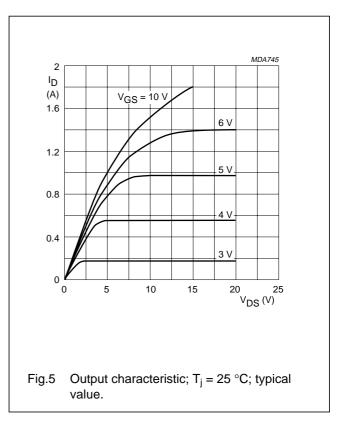
$T_{j} = 25  ^{\circ}\text{C unless otherwise specified}$ Drain-source breakdown voltage $I_{D} = 10  \mu\text{A};  V_{GS} = 0 \qquad \qquad V_{(BR)DSS} \qquad \text{min.} \qquad 200  \text{ V}$ Drain-source leakage current $V_{DS} = 160  \text{V};  V_{GS} = 0 \qquad \qquad I_{DSS} \qquad \text{max.} \qquad 1.0   \mu\text{A}$ $V_{DS} = 60  \text{V};  V_{GS} = 0 \qquad \qquad I_{DSS} \qquad \text{max.} \qquad 200  \text{ nA}$ Gate-source leakage current $\pm V_{GS} = 20  \text{V};  V_{DS} = 0 \qquad \qquad \pm I_{GSS} \qquad \text{max.} \qquad 100  \text{ nA}$ Gate threshold voltage $I_{D} = 1  \text{mA};  V_{DS} = V_{GS} \qquad \qquad V_{GS(th)} \qquad \begin{array}{c} \text{min.} \qquad 0.8  \text{ V} \\ \text{max.} \qquad 2.8  \text{ V} \end{array}$
$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Drain-source leakage current $V_{DS} = 160 \text{ V; } V_{GS} = 0 \\ V_{DS} = 60 \text{ V; } V_{GS} = 0 \\ V_{DS} = 60 \text{ V; } V_{GS} = 0 \\ \text{Gate-source leakage current} \\ \pm V_{GS} = 20 \text{ V; } V_{DS} = 0 \\ \text{Gate threshold voltage} \\ I_D = 1 \text{ mA; } V_{DS} = V_{GS} \\ \text{V} \\ \text{Max.} \\ \text{In the source leakage current} \\ \text{Max.} \\ \text{In the source leakage current} \\ \text{Max.} \\ \text{Max.}$
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$V_{DS} = 60 \text{ V; } V_{GS} = 0 \\ \text{Gate-source leakage current} \\ \pm V_{GS} = 20 \text{ V; } V_{DS} = 0 \\ \text{Gate threshold voltage} \\ I_D = 1 \text{ mA; } V_{DS} = V_{GS} \\ \text{Max.} \\ 200 \text{ nA} \\ \pm I_{GSS} \\ \text{max.} \\ 100 \text{ nA} \\ \text{min.} \\ 0.8 \text{ V} \\ 2.8 \text{ V} \\ \text{max.} \\ 2.8 \text{ V}$
Gate-source leakage current $ \pm V_{GS} = 20 \text{ V; } V_{DS} = 0 \\ \text{Gate threshold voltage} \\ I_D = 1 \text{ mA; } V_{DS} = V_{GS} \\ \text{V} \\ \text{Max.} \\ \text{Solution} $
$ \pm V_{GS} = 20 \text{ V; } V_{DS} = 0 $ $ \pm I_{GSS} $ max. $ 100 \text{ nA} $ Gate threshold voltage $ I_D = 1 \text{ mA; } V_{DS} = V_{GS} $ $ V_{GS(th)} $ min. $ 0.8 \text{ V} $ $ 2.8 \text{ V} $
Gate threshold voltage $I_D = 1 \text{ mA; } V_{DS} = V_{GS} \\ V_{GS(th)} \\ \text{max.} \\ 0.8 \text{ V} \\ \text{max.} \\ 2.8 \text{ V}$
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$ $V_{GS(th)}$ $min.$ $max.$ $2.8 \text{ V}$
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$ $V_{GS(th)}$ max. 2.8 V
During a supply of the supply
Drain-source on-resistance
$I_D = 400 \text{ mA}; V_{GS} = 10 \text{ V}$ $R_{DS(on)}$ $R_{DS(on)}$ max. $4.5 \Omega$ $6.0 \Omega$
IIIax. 0.0 sz
Transfer admittance
$I_D = 400 \text{ mA}; V_{DS} = 25 \text{ V}$ $ Y_{fs} $ $\frac{\text{min.}}{\text{typ.}}$ $\frac{200 \text{ mS}}{350 \text{ mS}}$
typ. ood me
Input capacitance at f = 1 MHz
$V_{DS} = 25 \text{ V}; V_{GS} = 0$ $C_{iss} \qquad typ. \qquad 45 \text{ pF}$ $max. \qquad 60 \text{ pF}$
max. oo pi
Output capacitance at f = 1 MHz
$V_{DS} = 25 \text{ V}; V_{GS} = 0$
παλ. 25 βι
Feedback capacitance at f = 1 MHz
$V_{DS} = 25 \text{ V}; V_{GS} = 0$ $C_{rss} \qquad \text{typ.} \qquad 3.5 \text{ pF} \\ \text{max.} \qquad 10 \text{ pF}$
παλ. το ρι
Switching times (see Figs 2 and 3)
$I_D = 250 \text{ mA}; V_{DD} = 50 \text{ V}; V_{GS} = 0 \text{ to } 10 \text{ V}$ ton typ. 5 pF max. 10 pF
παλ. 10 με
typ. 15 ns
t <sub>off</sub> max. 20 ns

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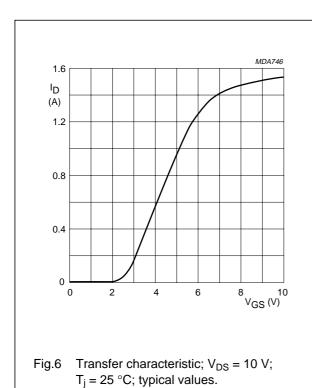






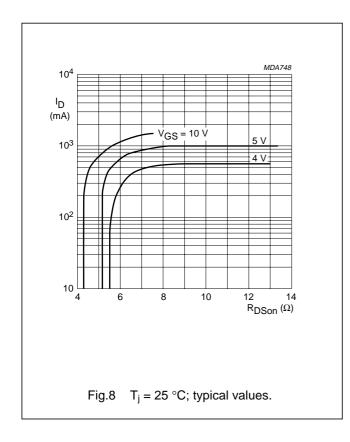


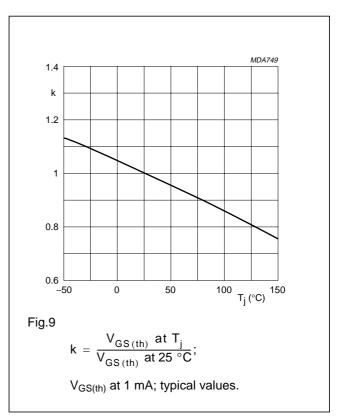
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160 C (pF) 120 C iss C coss C rss VDS (V)

Fig.7 Capacitance as a function of drain-source voltage;  $V_{GS}$  = 0; f = 1 MHz;  $T_j$  = 25 °C; typical values.





**BSP121** 

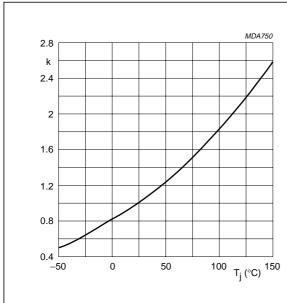


Fig.10  $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25 \degree C};$ 

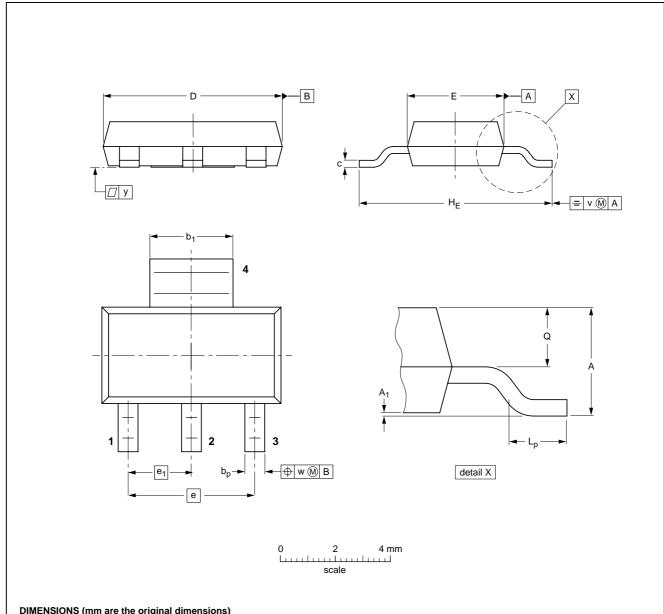
at 400 mA/10 V; typical values.

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#### **PACKAGE OUTLINE**

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

**SOT223** 



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UNIT	A	A <sub>1</sub>	bp	b <sub>1</sub>	С	D	E	е	e <sub>1</sub>	HE	Lp	Q	v	w	у	
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1	

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT223					<del>96-11-11</del> 97-02-28	

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#### **DEFINITIONS**

Data sheet status				
Objective specification	This data sheet contains target or goal specifications for product development.			
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.			
Product specification	Product specification This data sheet contains final product specifications.			
Application information				
Where application information is given, it is advisory and does not form part of the specification.				

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# N-channel enhancement mode vertical D-MOS transistor

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**NOTES** 

# N-channel enhancement mode vertical D-MOS transistor

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